MT7628 DATASHEET

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Overview

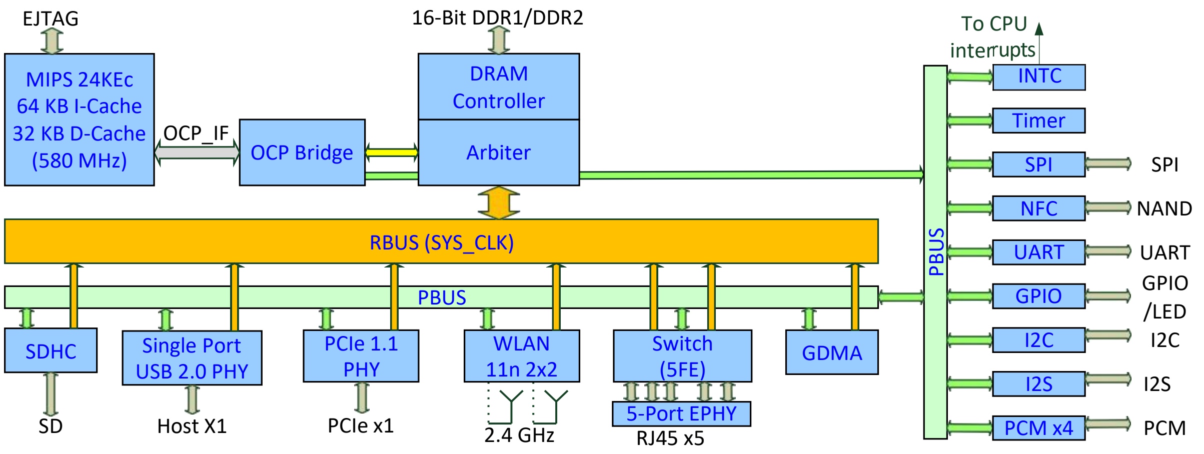
The MT7628 router-on-a-chip includes an 802.11n MAC and baseband, a 2.4 GHz radio and FEM, a 580 MHz MIPS® 24K™ CPU core, a 5-port 10/100 fast ethernet switch. The MT7628 includes everything needed to build an AP router from a single chip. The embedded high performance CPU can process advanced applications effortlessly, such as routing, security and VoIP. The MT7628 also includes a selection of interfaces to support a variety of applications, such as a USB port for accessing external storage.

Applications:
- Routers
- NAS devices
- Dual band concurrent routers

Features

- Embedded MIPS24KEc (580 MHz) with 64 KB I-Cache and 32 KB D-Cache
- 2T2R 2.4 GHz with 300 Mbps PHY data rate
- Legacy 802.11b/g and HT 802.11n modes
- 20/40 MHz channel bandwidth
- Legacy 802.11b/g and HT 802.11n modes
- Reverse Data Grant (RDG)
- Maximal Ratio Combining (MRC)
- Space Time Block Coding (STBC)
- MCM 8 Mbytes DDR1 KGD (MT7628KN)
- 16-bit DDR1/2 up to 128/256 Mbytes (MT7628NN/KN)
- SPI/SD-XC/eMMC
- x1 USB 2.0 Host, x1 PCIe Root Complex
- 5-port 10/100 FE PHY
- Internet Of Thing
- An optimized PMU
- Green AP
  - Intelligent Clock Scaling (exclusive)
  - DDRII: ODT off, Self-refresh mode
- I2C, I2S, SPI, PCM, UART, JTAG, GPIO
- 16 Multiple BSSID
- WEP64/128, TKIP, AES, WPA, WPA2, WAPI
- QoS: WMM, WMM-PS
- WPS: PBC, PIN
- Voice Enterprise: 802.11k+r
- AP Firmware: Linux 2.6 SDK, eCOS with IPv6

Functional Block Diagram



Ordering Information

Part Number	Package (Green/RoHS Compliant)
MT7628NN	DR-QFN 156 pin (12 mm x 12 mm)
MT7628KN	DR-QFN 120 pin (10 mm x 10 mm)

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1. Main Features

The following table covers the main features offered by the MT7628KN and MT7628NN. Overall, the MT7628KN supports the requirements of an entry-level AP/router, while the more advanced MT7628NN supports a number of interfaces together with a large maximum RAM capacity.

Features	MT7628KN	MT7628NN
CPU	MIPS24KEc (580 MHz)	MIPS24KEc (580 MHz)
Total DMIPs	580 x 1.6 DMIPs	580 x 1.6 DMIPs
I-Cache, D-Cache	64 KB, 32 KB	64 KB, 32 KB
L2 Cache	n/a	n/a
Memory		
DRAM Device width support	16 bits	16 bits
DDR1	64 Mb (MCM), 193 MHz	2 Gb, 193 MHz
DDR2	n/a	2 Gb, 193 MHz
SPI Flash	3B addr mode (max 128Mbit) 4B addr mode (max 512Mbit)	3B addr mode (max 128Mbit) 4B addr mode (max 512Mbit)
SD	n/a	SD-XC (class 10)
RF	2T2R 802.11n 2.4 GHz	2T2R 802.11n 2.4 GHz
PCIe	1	1
USB 2.0	1	1
Switch	5p FE SW	5p FE SW
I2S	1	1
PCM	1	1
I2C	1	1
UART	2 (Lite)	2 (Lite)
JTAG	1	1
Package	DR-QFN120- 10 mm x 10 mm	DR-QFN156- 12 mm x 12 mm

Table 1-1 Main Features

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2. Pins

2.1 MT7628NN DR-QFN (12 mm x 12 mm) 156-Pin Package Diagram

2.1.1 Up-left side

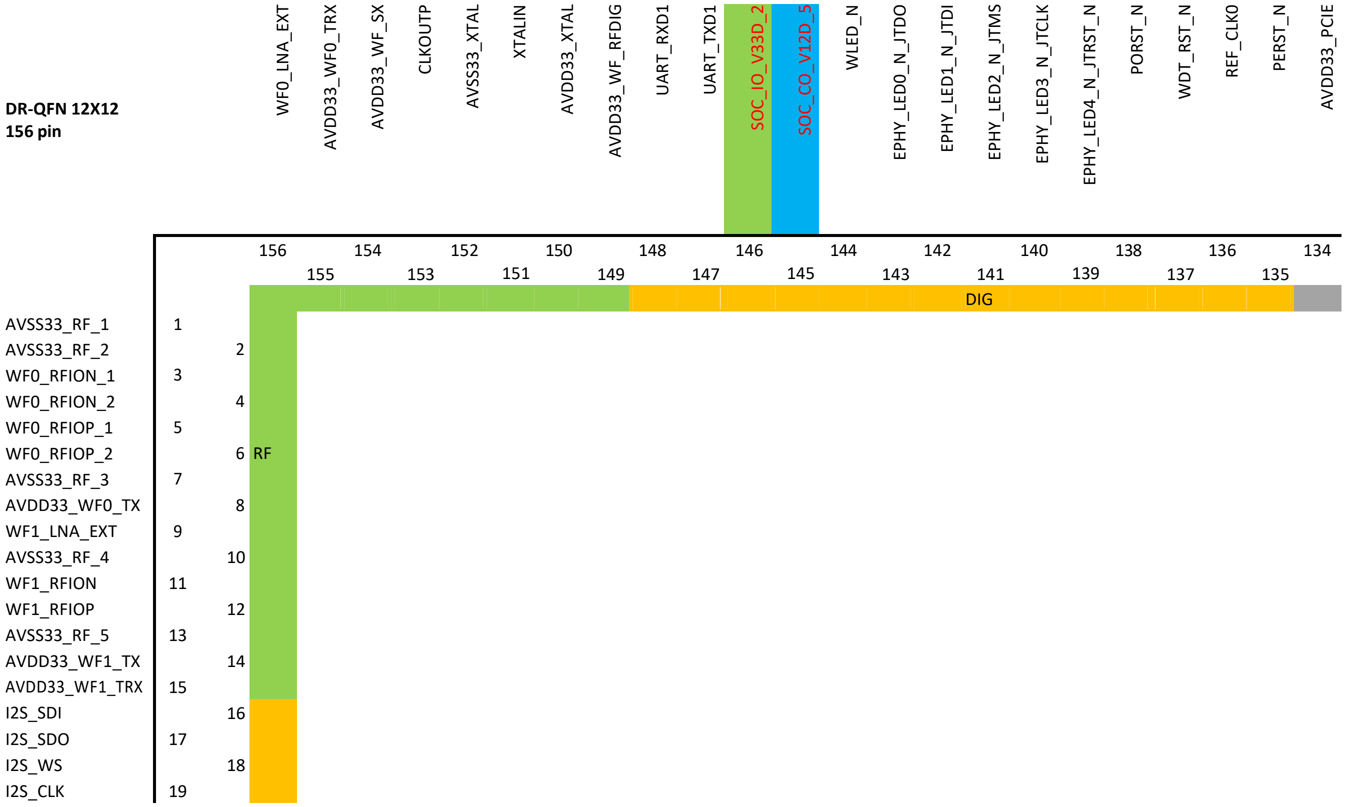

Figure 2-1 MT7628NN DR-QFN Pin Diagram (up-left view)

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2.1.2 Down-left side

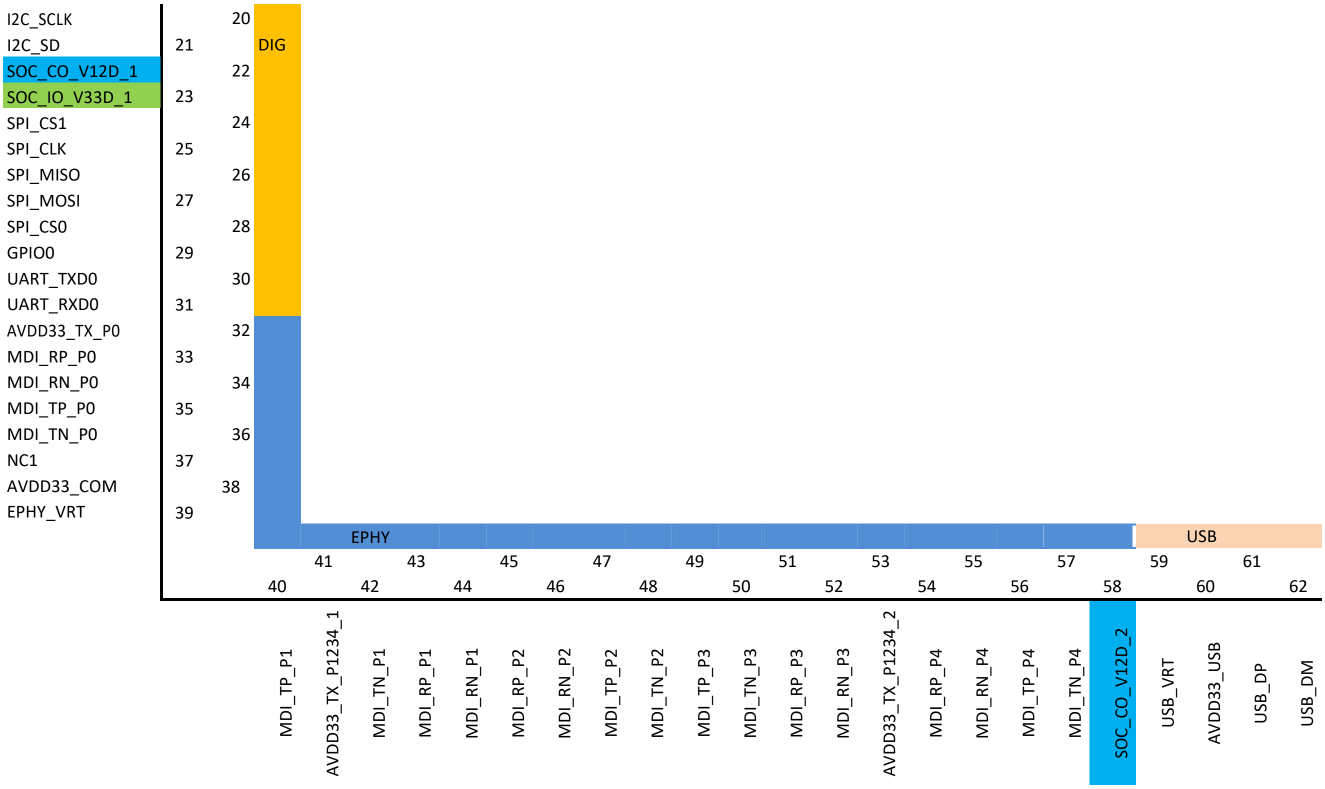

Figure 2-2 MT7628NN DR-QFN Pin Diagram (down-left view)

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2.1.3 Down-right side

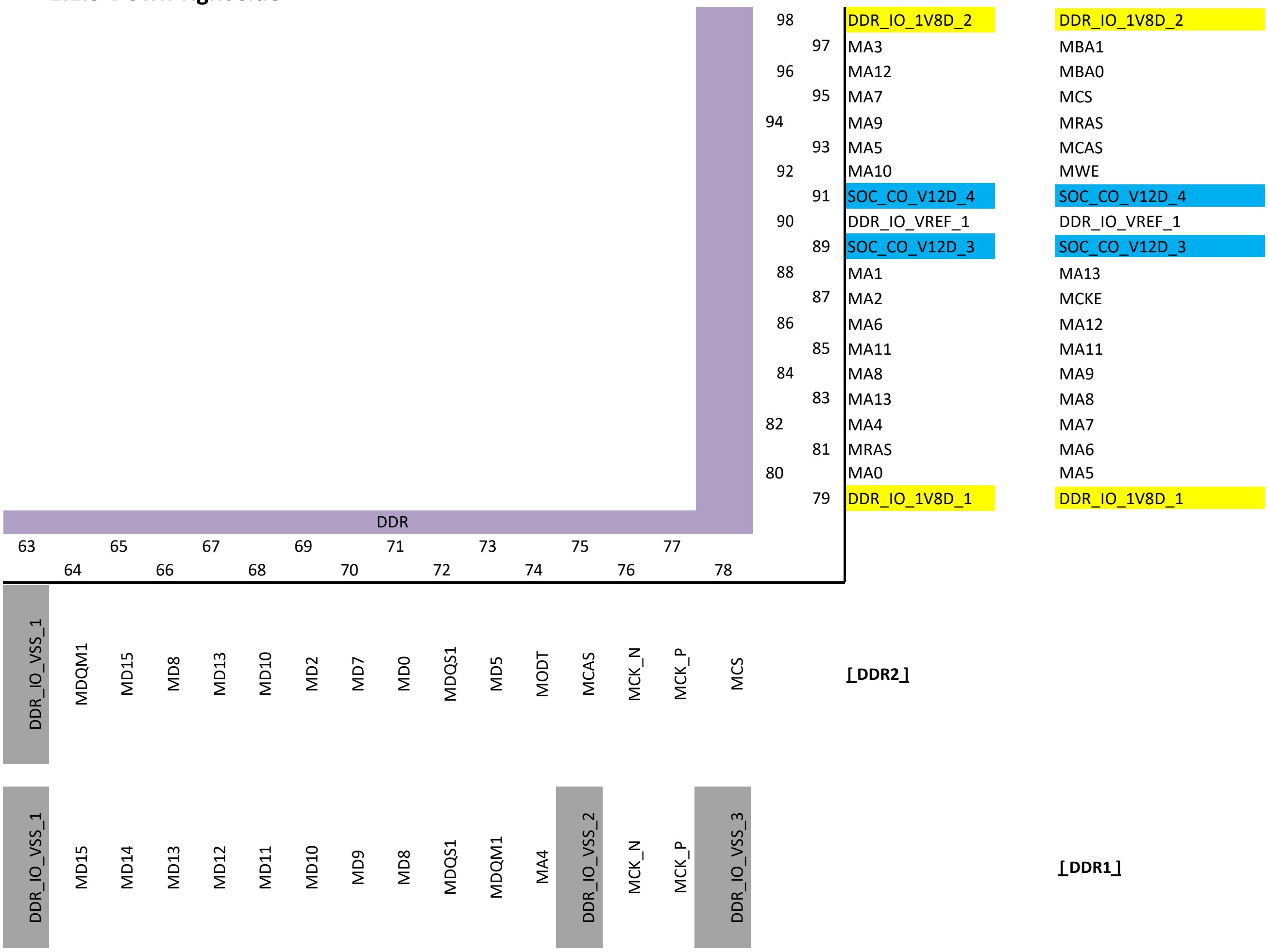

Figure 2-3 MT7628NN DR-QFN Pin Diagram (down-right view)

Note: DR-QFN support DDR1 and DDR2 pin shuffle depend on the bootstrap.

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2.1.4 Up-right side

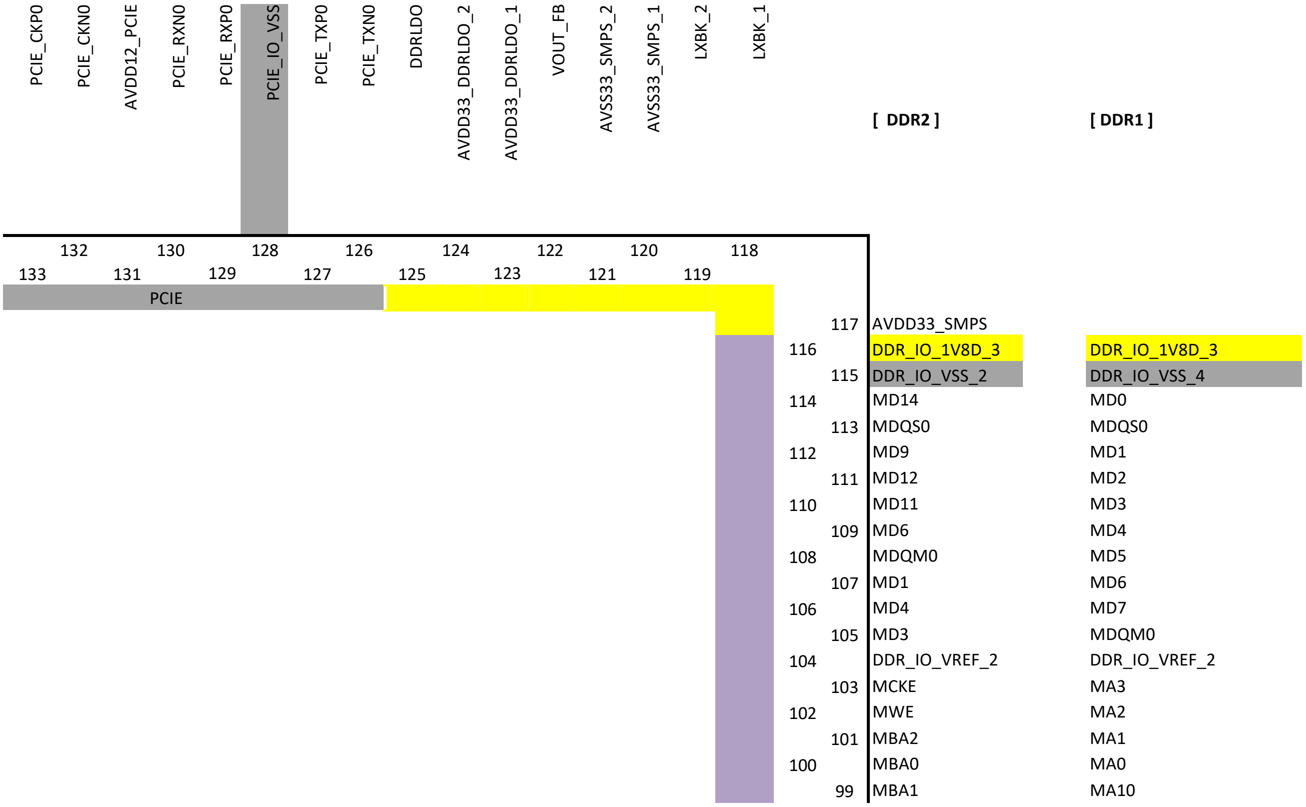

Figure 2-4 MT7628NN DR-QFN Pin Diagram (up-right view)

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2.1.5 Pin Description

Pins	Name	Type	Driv.	Description
RF				
3,4	WF0_RFION_1 WF0_RFION_2	A		WF0 main path RF I/O
5,6	WF0_RFIOP_1 WF0_RFIOP_2	A		WF0 main path RF I/O
11	WF1_RFION	A		WF1 main path RF I/O
12	WF1_RFIOP	A		WF1 main path RF I/O
9	WF1_LNA_EXT	A		WF1 aux. path LNA input
156	WF0_LNA_EXT	A		WF0 aux. path LNA input
151	XTALIN	I		Crystal oscillator input
153	CLKOUTP	O		XO reference clock output
152	AVDD33_XTAL	P		3.3V XTAL Power Supply Pin
150	AVSS33_XTAL	G		3.3V XTAL Ground Pin
8	AVDD33_WF0_TX	P		3.3V RF Channel 0 Suppoly Power
14	AVDD33_WF1_TX	P		3.3V RF Channel 1 Suppoly Power
15	AVDD33_WF1_TRX	P		1.65V to 3.3V RF Channel 1 Suppoly Power
149	AVDD33_WF_RFDIG	P		1.65V to 3.3V RF DIG and AFE Suppoly Power
154	AVDD33_WF_SX	P		1.65V to 3.3V RF Supply Power
155	AVDD33_WF0_TRX	P		1.65V to 3.3V RF Channel 0 Suppoly Power
1,2 7,13	AVSS33_RF	G		3.3V RF Shielding Ground Pin
WLAN LED				
144	WLED_N	O	4 mA	WLAN Activity LED
UART0 Lite				
31	RXD0	I	4 mA	UART0 Lite RXD
30	TXD0	O, IPD	4 mA	UART0 Lite TXD
UART1 Lite				
147	TXD1	O, IPU	4 mA	UART1 Lite TXD
148	RXD1	I	4 mA	UART1 Lite RXD
I2S				
16	I2S_SDI	O	4 mA	I2S data input
17	I2S_SDO	I/O, IPD	4 mA	I2S data output
18	I2S_WS	O	4 mA	I2S word select
19	I2S_CLK	I/O	4 mA	I2S clock
I2C				
21	I2C_SD		4 mA	I2C Data

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Pins	Name	Type	Driv.	Description
20	I2C_SCLK	I/O	4 mA	I2C Clock
SPI				
26	SPI_MISO	I/O	4 mA	SPI Master input/Slave output
27	SPI_MOSI	I/O, IPD	4 mA	SPI Master output/Slave input
25	SPI_CLK	O, IPU	4 mA	SPI clock
28	SPI_CS0	O	4 mA	SPI chip select0
24	SPI_CS1	O, IPD	4 mA	SPI chip select1
GPIO				
29	GPIO0	I/O, IPD	4 mA	General Purpose I/O
5-Port EPHY				
143	EPHY_LED0 _N_JTDO	I/O	4 mA	10/100 PHY Port #0 activity LED, JTAG_TDO
142	EPHY_LED1 _N_JTDI	I/O	4 mA	10/100 PHY Port #1 activity LED, JTAG_TDI
141	EPHY_LED2 _N_JTMS	I/O	4 mA	10/100 PHY Port #2 activity LED, JTAG_TMS
140	EPHY_LED3 _N_JTCLK	I/O	4 mA	10/100 PHY Port #3 activity LED, JTAG_CLK
139	EPHY_LED4 _N_JTRST_N	I/O,	4 mA	10/100 PHY Port #4 activity LED, JTAG_TRST_N
39	EPHY_VRT	A		Connect to an external resistor to provide accurate bias current
33	MDI_RP_P0	A		10/100 PHY Port #0 RXN
34	MDI_RN_P0	A		10/100 PHY Port #0 RXP
35	MDI_TP_P0	A		10/100 PHY Port #0 TXN
36	MDI_TN_P0	A		10/100 PHY Port #0 TXP
40	MDI_TP_P1	A		10/100 PHY Port #1 RXN
42	MDI_TN_P1	A		10/100 PHY Port #1 RXP
43	MDI_RP_P1	A		10/100 PHY Port #1 TXN
44	MDI_RN_P1	A		10/100 PHY Port #1 TXP
45	MDI_RP_P2	A		10/100 PHY Port #2 RXN
46	MDI_RN_P2	A		10/100 PHY Port #2 RXP
47	MDI_TP_P2	A		10/100 PHY Port #2 TXN
48	MDI_TN_P2	A		10/100 PHY Port #2 TXP
49	MDI_TP_P3	A		10/100 PHY Port #3 RXN
50	MDI_TN_P3	A		10/100 PHY Port #3 RXP
51	MDI_RP_P3	A		10/100 PHY Port #3 TXN
52	MDI_RN_P3	A		10/100 PHY Port #3 TXP
54	MDI_RP_P4	A		10/100 PHY Port #4 RXN
55	MDI_RN_P4	A		10/100 PHY Port #4 RXP
56	MDI_TP_P4	A		10/100 PHY Port #4 TXN

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Pins	Name	Type	Driv.	Description
57	MDI_TN_P4	A		10/100 PHY Port #4 TXP
32	AVDD33_TX_P0	P		3.3V Supply Power for P0
38	AVDD33_COM	P		3.3V Supply Power for EPHY COM
41	AVDD33_TX_P1234_1 AVDD33_TX_P1234_2	P		3.3V Supply Power for P1 ~ P4
Misc.				
136	REF_CLKO	O, IPD	4 mA	Reference Clock Ouptut
138	PORST_N	I, IPU	4 mA	Power on reset
137	WDT_RST_N	O	4 mA	Watchdog timeout reset
USB PHY				
129	AVDD33_USB	P		3.3 V USB PHY analog power supply
130	USB _VRT	I/O		Connect to an external 5.1 kΩ resistor for band-gap reference circuit
62	USB_DM	I/O		USB Port0 data pin Data-
61	USB _DP	I/O		USB Port0 data pin Data+
PCIe PHY				
135	PERST_N	O, IPD	4mA	PCIe device reset
134	AVDD12_PCIE	P		1.2 V PCIE PHY digital power supply
129	AVDD33_PCIE	P		3.3 V USB PHY analog power supply
128	PCIE_IO_VSS	P		PCIE PHY Ground Pin
133	PCIE_CKP0	I/O		External reference clock output (positive)
132	PCIE_CKN0	I/O		External reference clock output (negative)
127	PCIE_TXP0	I/O		PCIe0 differential transmit TX -
126	PCIE_TXN0	I/O		PCIe0 differential transmit TX -
129	PCIE_TXP0	I/O		PCIe0 differential receiver RX -
130	PCIE_TXN0	I/O		PCIe0 differential receiver RX -
DDR2				
65	MD15	I/O	8 mA	DDR2 Data bit #15
114	MD14	I/O	8 mA	DDR2 Data bit #14
67	MD13	I/O	8 mA	DDR2 Data bit #13
111	MD12	I/O	8 mA	DDR2 Data bit #12
110	MD11	I/O	8 mA	DDR2 Data bit #11
68	MD10	I/O	8 mA	DDR2 Data bit #10
112	MD9	I/O	8 mA	DDR2 Data bit #9
66	MD8	I/O	8 mA	DDR2 Data bit #8
70	MD7	I/O	8 mA	DDR2 Data bit #7
109	MD6	I/O	8 mA	DDR2 Data bit #6

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Pins	Name	Type	Driv.	Description
73	MD5	I/O	8 mA	DDR2 Data bit #5
106	MD4	I/O	8 mA	DDR2 Data bit #4
105	MD3	I/O	8 mA	DDR2 Data bit #3
69	MD2	I/O	8 mA	DDR2 Data bit #2
107	MD1	I/O	8 mA	DDR2 Data bit #1
71	MD0	I/O	8 mA	DDR2 Data bit #0
83	MA13	O	8 mA	DDR2 Address bit #13
96	MA12	O	8 mA	DDR2 Address bit #12
85	MA11	O	8 mA	DDR2 Address bit #11
92	MA10	O	8 mA	DDR2 Address bit #10
94	MA9	O	8 mA	DDR2 Address bit #9
84	MA8	O	8 mA	DDR2 Address bit #8
95	MA7	O	8 mA	DDR2 Address bit #7
86	MA6	O	8 mA	DDR2 Address bit #6
93	MA5	O	8 mA	DDR2 Address bit #5
82	MA4	O	8 mA	DDR2 Address bit #4
97	MA3	O	8 mA	DDR2 Address bit #3
87	MA2	O	8 mA	DDR2 Address bit #2
88	MA1	O	8 mA	DDR2 Address bit #1
80	MA0	O	8 mA	DDR2 Address bit #0
101	MBA2	O	8 mA	DDR2 MBA #2
99	MBA1	O	8 mA	DDR2 MBA #1
100	MBA0	O	8 mA	DDR2 MBA #0
74	MODT	O	8 mA	DDR2 ODT
81	MRAS	O	8 mA	DDR2 MRAS_N
75	MCAS	O	8 mA	DDR2 MCAS_N
102	MWE	O	8 mA	DDR2 MWE_N
77	MCK_P	O	8 mA	DDR2 MCK_P
76	MCK_N	O	8 mA	DDR2 MCK_N
64	MDQM1	O	8 mA	DDR2 MDQM#1
108	MDQM0	O	8 mA	DDR2 MDQM#0
78	MCS	O	8 mA	DDR2 MCS
72	MDQS1	I/O	8 mA	DDR2 MDQS#1
113	MDQS0	I/O	8 mA	DDR2 MDQS#0
103	MCKE	O	8 mA	DDR2 MCKE
63 115	DDR_IO_VSS_1 DDR_IO_VSS_2	G		DDR IO Ground pins

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Pins	Name	Type	Driv.	Description
79 98 116	DDR_IO_1V8D_1 DDR_IO_1V8D_2 DDR_IO_1V8D_3	P		DDR io Supply power
90 104	DDR_IO_VREF_1 DDR_IO_VREF_2	A		DDR reference voltage
DDR1				
64	MD15	I/O	8 mA	DDR1 Data bit #15
65	MD14	I/O	8 mA	DDR1 Data bit #14
66	MD13	I/O	8 mA	DDR1 Data bit #13
67	MD12	I/O	8 mA	DDR1 Data bit #12
68	MD11	I/O	8 mA	DDR1 Data bit #11
69	MD10	I/O	8 mA	DDR1 Data bit #10
70	MD9	I/O	8 mA	DDR1 Data bit #9
71	MD8	I/O	8 mA	DDR1 Data bit #8
106	MD7	I/O	8 mA	DDR1 Data bit #7
107	MD6	I/O	8 mA	DDR1 Data bit #6
108	MD5	I/O	8 mA	DDR1 Data bit #5
109	MD4	I/O	8 mA	DDR1 Data bit #4
110	MD3	I/O	8 mA	DDR1 Data bit #3
111	MD2	I/O	8 mA	DDR1 Data bit #2
112	MD1	I/O	8 mA	DDR1 Data bit #1
114	MD0	I/O	8 mA	DDR1 Data bit #0
88	MA13	O	8 mA	DDR1 Address bit #13
86	MA12	O	8 mA	DDR1 Address bit #12
85	MA11	O	8 mA	DDR1 Address bit #11
99	MA10	O	8 mA	DDR1 Address bit #10
84	MA9	O	8 mA	DDR1 Address bit #9
83	MA8	O	8 mA	DDR1 Address bit #8
82	MA7	O	8 mA	DDR1 Address bit #7
81	MA6	O	8 mA	DDR1 Address bit #6
80	MA5	O	8 mA	DDR1 Address bit #5
74	MA4	O	8 mA	DDR1 Address bit #4
103	MA3	O	8 mA	DDR1 Address bit #3
102	MA2	O	8 mA	DDR1 Address bit #2
101	MA1	O	8 mA	DDR1 Address bit #1
100	MA0	O	8 mA	DDR1 Address bit #0
97	MBA1	O	8 mA	DDR1 MBA #1

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Pins	Name	Type	Driv.	Description
96	MBA0	O	8 mA	DDR1 MBA #0
94	MRAS	O	8 mA	DDR1 MRAS_N
93	MCAS	O	8 mA	DDR1 MCAS_N
92	MWE	O	8 mA	DDR1 MWE_N
77	MCK_P	O	8 mA	DDR1 MCK_P
76	MCK_N	O	8 mA	DDR1 MCK_N
73	MDQM1	O	8 mA	DDR1 MDQM#1
105	MDQM0	O	8 mA	DDR1 MDQM#0
95	MCS	O	8 mA	DDR1 MCS
72	MDQS1	I/O	8 mA	DDR1 MDQS#1
113	MDQS0	I/O	8 mA	DDR1 MDQS#0
87	MCKE	O	8 mA	DDR1 MCKE
63 75 78 115	DDR_IO_VSS_1 DDR_IO_VSS_2 DDR_IO_VSS_3 DDR_IO_VSS_4	G		DDR IO Ground pins
79 98 116	DDR_IO_1V8D_1 DDR_IO_1V8D_2 DDR_IO_1V8D_3	P		DDR IO Supply power
90 104	DDR_IO_VREF_1 DDR_IO_VREF_2	A		DDR reference voltage
PMU				
118 119	LXBK_1 LXBK_2	O		Buck Switching node
122	VOUT_FB	A		Buck vout feedback pin
59	AVDD33_SMPS	P		Buck 3.3V Supply power
120 121	AVSS33_SMPS_1 AVSS33_SMPS_2	G		Buck Gound pin
123 124	AVDD33_DDRLDO_1 AVDD33_DDRLDO_2	G		DDRLDO 3.3V Supply power
56	DDRLDO	O		DDRLDO 1.8V/2.5V output voltage
Power				
23 146	SOC_IO_V33D_1 SOC_IO_V33D_2	P		3.3 V digital I/O power supply
22 58 89 91 145	SOC_CO _V12D_1 SOC_CO _V12D_2 SOC_CO _V12D_3 SOC_CO _V12D_4 SOC_CO _V12D_5	P		1.2 V digital core power supply
EPAD	GND	G		Ground pin

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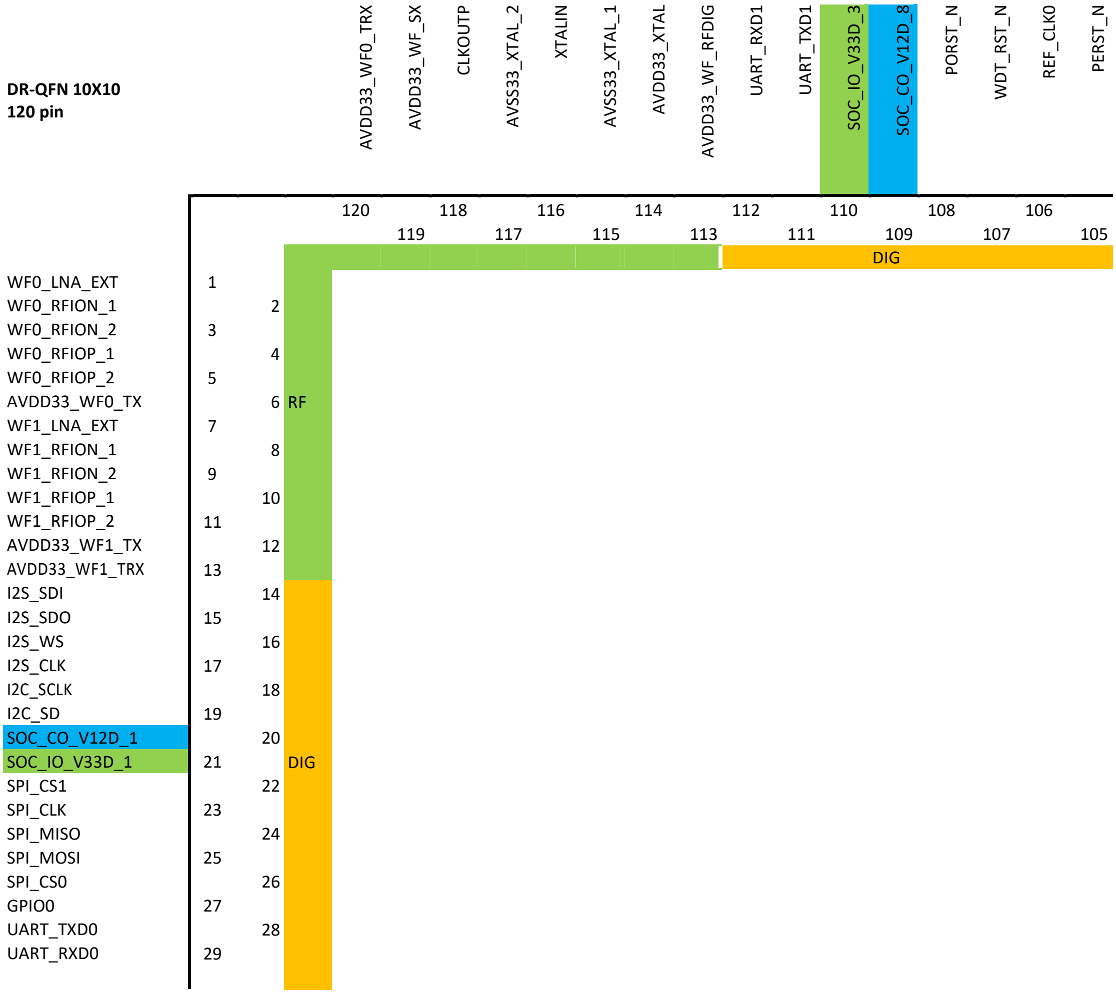
Pins	Name	Type	Driv.	Description
Total: 156 pins				

Note:

IPD : Internal pull-down
IPU : Internal pull-up
I : Input
O : Output
IO : Bi-directional
P : Power
G : Ground
NC : Not connected

2.2 MT7628KN DR-QFN (10 mm x 10 mm) 120-Pin Package Diagram

2.2.1 Left side vie



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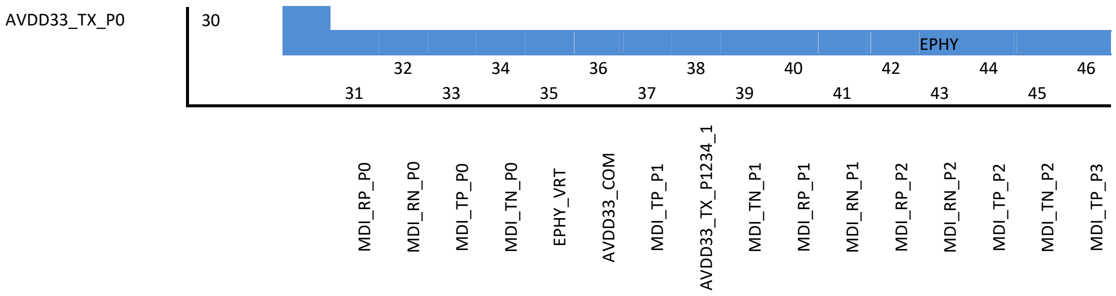

Figure 2-5 MT7628KN DR-QFN Pin Diagram (left view)

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2.2.2 Right side view

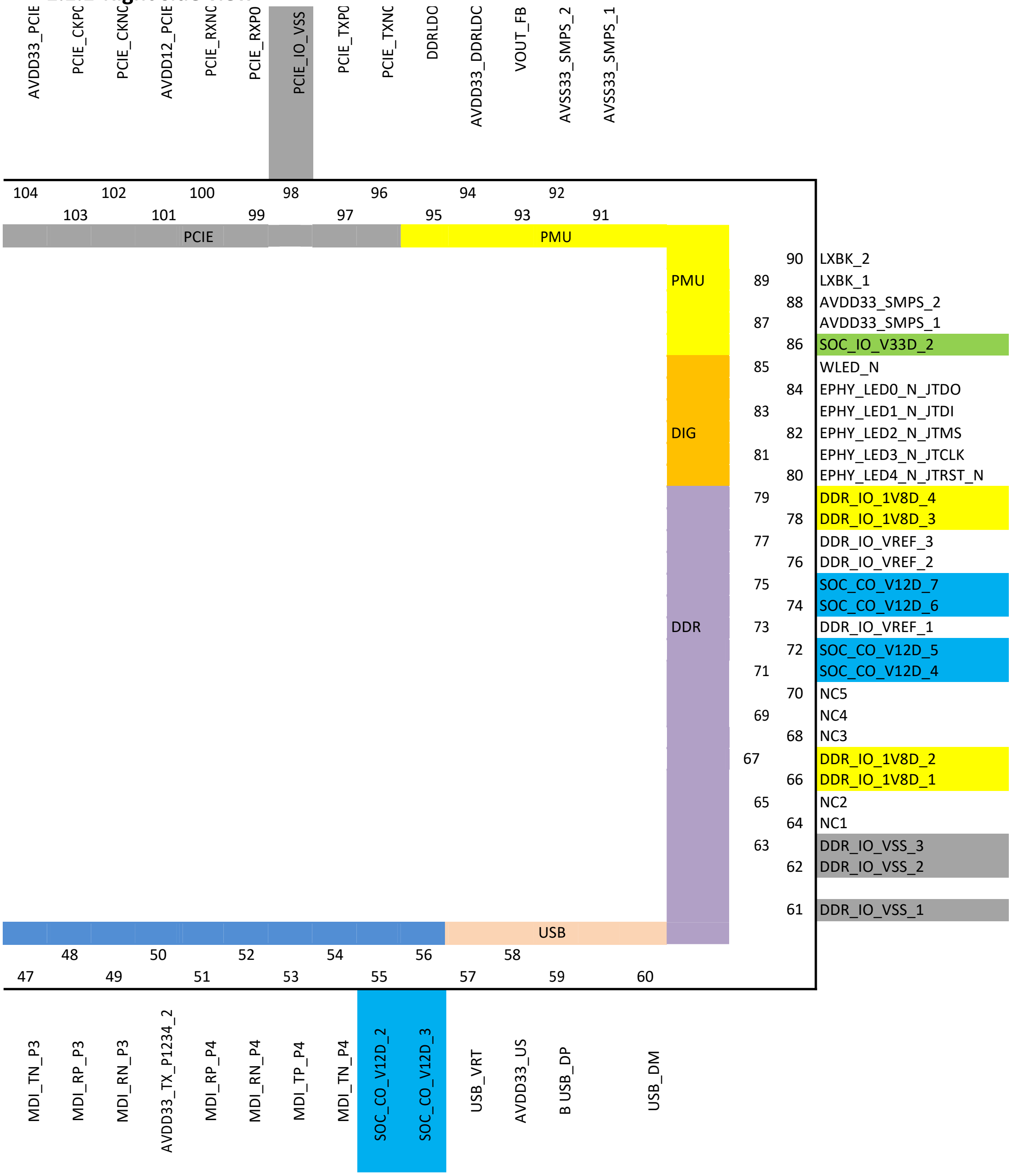

Figure 2-6 MT7628KN DR-QFN Pin Diagram (right side view)

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2.2.3 Pin Description

Pins	Name	Type	Driv.	Description
RF				
2 3	WF0_RFION_1 WF0_RFION_2	A		WF0 main path RF I/O
4 5	WF0_RFIOP_1 WF0_RFIOP_2	A		WF0 main path RF I/O
8 9	WF1_RFION_1 WF1_RFION_2	A		WF1 main path RF I/O
10 11	WF1_RFIOP_1 WF1_RFIOP_2	A		WF1 main path RF I/O
7	WF1_LNA_EXT	A		WF1 aux. path LNA input
1	WF0_LNA_EXT	A		WF0 aux. path LNA input
116	XTALIN	I		Crystal oscillator input
118	CLKOUTP	O		XO reference clock output
114	AVDD33_XTAL	P		3.3V XTAL Power Supply Pin
115 117	AVS33_XTAL_1 AVS33_XTAL_2	G		3.3V XTAL Ground Pin
6	AVDD33_WF0_TX	P		3.3V RF Channel 0 Suppoly Power
12	AVDD33_WF1_TX	P		3.3V RF Channel 1 Suppoly Power
13	AVDD33_WF1_TRX	P		1.65V to 3.3V RF Channel 1 Suppoly Power
113	AVDD33_WF_RFDIG	P		1.65V to 3.3V RF DIG and AFE Suppoly Power
119	AVDD33_WF_SX	P		1.65V to 3.3V RF Supply Power
120	AVDD33_WF0_TRX	P		1.65V to 3.3V RF Channel 0 Suppoly Power
WLAN LED				
85	WLED_N	O	4 mA	WLAN Activity LED
UART0 Lite				
28	TXD0	O, IPD	4 mA	UART0 Lite TXD
29	RXD0	I		UART0 Lite RXD
UART1 Lite				
111	TXD1	O, IPU	4 mA	UART1 Lite TXD
112	RXD1	I		UART1 Lite RXD
I2S				
14	I2S_SDI	I/O	4 mA	I2S data input
15	I2S_SDO	O, IPD	4 mA	I2S data output
16	I2S_WS	O	4 mA	I2S word select
17	I2S_CLK	I/O	4 mA	I2S clock
I2C				
19	I2C_SD	I/O	4 mA	I2C Data

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Pins	Name	Type	Driv.	Description
18	I2C_SCLK	I/O	4 mA	I2C Clock
SPI				
24	SPI_MISO	I/O	4 mA	SPI Master input/Slave output
25	SPI_MOSI	I/O, IPD	4 mA	SPI Master output/Slave input
22	SPI_CLK	O, IPU	4 mA	SPI clock
26	SPI_CS0	O	4 mA	SPI chip select0
22	SPI_CS1	O, IPD	4 mA	SPI chip select1
GPIO				
27	GPIO0	I/O, IPD	4 mA	General Purpose I/O
5-Port EPHY				
84	EPHY_LED0 _N_JTDO	I/O	4 mA	10/100 PHY Port #0 activity LED, JTAG_TDO
83	EPHY_LED1 _N_JTDI	I/O	4 mA	10/100 PHY Port #1 activity LED, JTAG_TDI
82	EPHY_LED2 _N_JTMS	I/O	4 mA	10/100 PHY Port #2 activity LED, JTAG_TMS
81	EPHY_LED3 _N_JTCLK	I/O	4 mA	10/100 PHY Port #3 activity LED, JTAG_CLK
80	EPHY_LED4 _N_JTRST_N	I/O,	4 mA	10/100 PHY Port #4 activity LED, JTAG_TRST_N
35	EPHY_VRT	A		Connect to an external resistor to provide accurate bias current
31	MDI_RP_P0	A		10/100 PHY Port #0 RXN
32	MDI_RN_P0	A		10/100 PHY Port #0 RXP
33	MDI_TP_P0	A		10/100 PHY Port #0 TXN
34	MDI_TN_P0	A		10/100 PHY Port #0 TXP
37	MDI_TP_P1	A		10/100 PHY Port #1 RXN
39	MDI_TN_P1	A		10/100 PHY Port #1 RXP
40	MDI_RP_P1	A		10/100 PHY Port #1 TXN
41	MDI_RN_P1	A		10/100 PHY Port #1 TXP
42	MDI_RP_P2	A		10/100 PHY Port #2 RXN
43	MDI_RN_P2	A		10/100 PHY Port #2 RXP
44	MDI_TP_P2	A		10/100 PHY Port #2 TXN
45	MDI_TN_P2	A		10/100 PHY Port #2 TXP
46	MDI_TP_P3	A		10/100 PHY Port #3 RXN
47	MDI_TN_P3	A		10/100 PHY Port #3 RXP
48	MDI_RP_P3	A		10/100 PHY Port #3 TXN
49	MDI_RN_P3	A		10/100 PHY Port #3 TXP
51	MDI_RP_P4	A		10/100 PHY Port #4 RXN
52	MDI_RN_P4	A		10/100 PHY Port #4 RXP
53	MDI_TP_P4	A		10/100 PHY Port #4 TXN

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Pins	Name	Type	Driv.	Description
54	MDI_TN_P4	A		10/100 PHY Port #4 TXP
30	AVDD33_TX_P0	P		3.3V Supply Power for P0
36	AVDD33_COM	P		3.3V Supply Power for EPHY COM
38 50	AVDD33_TX_P1234_1 AVDD33_TX_P1234_2	P		3.3V Supply Power for P1 ~ P4
Misc.				
106	REF_CLKO	O, IPD	4 mA	Reference Clock Ouptut
108	PORST_N	I		Power on reset
107	WDT_RST_N	O	4 mA	Watchdog Reset
USB PHY				
58	AVDD33_USB	P		3.3 V USB PHY analog power supply
57	USB _VRT	A		Connect to an external 5.1 kΩ resistor for band-gap reference circuit
60	USB_DM	I/O		USB Port0 data pin Data-
59	USB _DP	I/O		USB Port0 data pin Data+
PCIe PHY				
105	PERST_N	O, IPD	4mA	PCIe device reset
98	PCIE_IO_VSS	G		PCIe Ground pin
101	AVDD12_PCIE	P		1.2 V PCIE PHY digital power supply
104	AVDD33_PCIE	P		3.3 V USB PHY analog power supply
103	PCIE_CKP0	O		External reference clock output (positive)
102	PCIE_CKN0	O		External reference clock output (negative)
97	PCIE_TXP0	I/O		PCIe0 differential transmit TX -
96	PCIE_TXN0	I/O		PCIe0 differential transmit TX -
99	PCIE_RXP0	I/O		PCIe0 differential receiver RX -
100	PCIE_RXN0	I/O		PCIe0 differential receiver RX -
PMU				
89 90	LXBK_1 LXBK_2	O		Buck Switching node
93	VOUT_FB	A		Buck vout feedback pin
87 88	AVDD33_SMPS_1 AVDD33_SMPS_2	P		Buck 3.3V Supply power
91 92	AVSS33_SMPS_1 AVSS33_SMPS_2	G		Buck Gound pin
94	AVDD33_DDRLDO	P		DDRLDO 3.3V Supply power
95	DDRLDO	O		DDRLDO 1.8V/2.5V output voltage
Power				

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Pins	Name	Type	Driv.	Description
21 86 110	SOC_IO_V33D_1 SOC_IO_V33D_2 SOC_IO_V33D_3	P		3.3 V digital I/O power supply
20 55 56 71 72 74 75 109	SOC_CO _V12D_1 SOC_CO _V12D_2 SOC_CO _V12D_3 SOC_CO _V12D_4 SOC_CO _V12D_5 SOC_CO _V12D_6 SOC_CO _V12D_7 SOC_CO _V12D_8	P		1.2 V digital core power supply
EPAD	GND	G		Ground pin
Total: 120 pins				

Note:
IPD : Internal pull-down
IPU : Internal pull-up
I : Input
O : Output
IO : Bi-directional
P : Power
G : Ground
NC : Not connected

2.3 Pin Sharing Schemes

Some pins are shared with GPIO to provide maximum flexibility for system designers. The MT7628 provides up to 41 GPIO pins. Users can configure GPIO1_MODE and GPIO2_MODE registers in the System Control block to specify the pin function, or they can use the registers specified below. For more information, see the Programmer's Guide. Unless specified explicitly, all the GPIO pins are in input mode after reset.

2.3.1 GPIO pin share scheme

I/O Pad Group	Normal Mode	GPIO Mode
UART1	UART_RXD1	GPIO#46
	UART_TXD1	GPIO#45
WLED_AN	WLED_N (7628AN)	GPIO#44
P0_LED_AN	EPHY_LED0_N_JTDO (7628AN)	GPIO#43
P1_LED_AN	EPHY_LED1_N_JTDI (7628AN)	GPIO#42
P2_LED_AN	EPHY_LED2_N_JTMS (7628AN)	GPIO#41
P3_LED_AN	EPHY_LED3_N_JTCLK (7628AN)	GPIO#40
P4_LED_AN	EPHY_LED4_N_JTRST_N (7628AN)	GPO#39
WDT	WDT_RST_N	GPO#38
REFCLK	REF_CLKO	GPIO#37

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I/O Pad Group	Normal Mode	GPIO Mode
PERST	PERST_N	GPIO#36
WLED_KN	WLED_N (7628KN)	GPIO#35
P0_LED_KN	EPHY_LED0_N_JTDO (7628KN)	GPIO#34
P1_LED_KN	EPHY_LED1_N_JTDI (7628KN)	GPIO#33
P2_LED_KN	EPHY_LED2_N_JTMS (7628KN)	GPIO#32
P3_LED_KN	EPHY_LED3_N_JTCLK (7628KN)	GPIO#31
P4_LED_KN	EPHY_LED4_N_JTRST_N (7628KN)	GPIO#30
SD	MDI_TN_P4	GPIO#29
	MDI_TP_P4	GPIO#28
	MDI_RN_P4	GPIO#27
	MDI_RP_P4	GPIO#26
	MDI_RN_P3	GPIO#25
	MDI_RP_P3	GPIO#24
	MDI_TN_P3	GPIO#23
	MDI_TP_P3	GPIO#22
UART2	MDI_TN_P2	GPIO#21
	MDI_TP_P2	GPIO#20
PWM1	MDI_RN_P2	GPO#19
PWM0	MDI_RP_P2	GPO#18
SPIS	MDI_RN_P1	GPIO#17
	MDI_RP_P1	GPIO#16
	MDI_TN_P1	GPO#15
	MDI_TP_P1	GPIO#14
UART0	UART_RXD0	GPIO#13
	UART_TXD0	GPIO#12
GPIO	GPIO0	GPIO#11
SPI	SPI_CS0	GPIO#10
	SPI_MISO	GPIO#9
	SPI_MOSI	GPIO#8
	SPI_CLK	GPIO#7
SPI_CS1	SPI_CS1	GPIO#6
I2C	I2C_SD	GPO#5
	I2C_SCLK	GPO#4
I2S	I2S_CLK	GPIO#3
	I2S_WS	GPIO#2
	I2S_SDO	GPIO#1
	I2S_SDI	GPO#0

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2.3.2 UART1 pin share scheme

Controlled by the UART1_MODE register.

Pin Name	2'b00 UART-Lite #1	2'b01 GPIO	2'b10 PWM	2'b11 TRX_SW
UART1_RXD	UART1_RXD	GPIO#46	PWM_CH1	
UART1_TXD	UART1_TXD	GPIO#45	PWM_CH0	

2.3.3 MT7628NN EPHY LED pin share scheme

Controlled by the P#_LED_AN_MODE registers

Pin Name	Bootstrapping (DBG_JTAG_MODE=1)	Bootstrapping (DBG_JTAG_MODE=0)	
		P4_LED_AN_MODE =2'b00	P4_LED_AN_MODE =2'b01
EPHY_LED4_N_JTRST_N	JTAG_RST_N	EPHY_LED4_N	GPIO#39
		P3_LED_AN_MODE =2'b00	P3_LED_AN_MODE =2'b01
EPHY_LED3_N_JTCLK	JTAG_CLK	EPHY_LED3_N	GPIO#40
		P2_LED_AN_MODE =2'b00	P2_LED_AN_MODE =2'b01
EPHY_LED2_N_JTMS	JTAG_TMS	EPHY_LED2_N	GPIO#41
		P1_LED_AN_MODE =2'b00	P1_LED_AN_MODE =2'b01
EPHY_LED1_N_JTDI	JTAG_TDI	EPHY_LED1_N	GPIO#42
		P0_LED_AN_MODE =2'b00	P0_LED_AN_MODE =2'b01
EPHY_LED0_N_JTDO	JTAG_TDO	EPHY_LED0_N	GPIO#43

2.3.4 MT7628NN WLAN LED pin share scheme

Controlled by the WLED_AN_MODE registers

Pin Name	2'b00	2'b01
WLED_N	WLED_N	GPIO#44

2.3.5 MT7628KN EPHY LED pin share scheme

Controlled by the P#_LED_KN_MODE registers

Pin Name	Bootstrapping (DBG_JTAG_MODE=1)	Bootstrapping (DBG_JTAG_MODE=0)	
		P4_LED_KN_MODE =2'b00	P4_LED_KN_MODE =2'b01

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Pin Name	Bootstrapping (DBG_JTAG_MODE=1)	Bootstrapping (DBG_JTAG_MODE=0)	
		P4_LED_KN_MODE =2'b00	P4_LED_KN_MODE =2'b01
EPHY_LED4_N_JTRST_N	JTAG_RST_N	EPHY_LED4_N	GPIO#30
		P3_LED_KN_MODE =2'b00	P3_LED_KN_MODE =2'b01
EPHY_LED3_N_JTCLK	JTAG_CLK	EPHY_LED3_N	GPIO#31
		P2_LED_KN_MODE =2'b00	P2_LED_KN_MODE =2'b01
EPHY_LED2_N_JTMS	JTAG_TMS	EPHY_LED2_N	GPIO#32
		P1_LED_KN_MODE =2'b00	P1_LED_KN_MODE =2'b01
EPHY_LED1_N_JTDI	JTAG_TDI	EPHY_LED1_N	GPIO#33
		P0_LED_KN_MODE =2'b00	P0_LED_KN_MODE =2'b01
EPHY_LED0_N_JTDO	JTAG_TDO	EPHY_LED0_N	GPIO#34

2.3.6 MT7628KN WLAN LED pin share scheme

Controlled by the WLED_KN_MODE registers

Pin Name	2'b00	2'b01
WLED_N	WLED_N	GPIO#35

2.3.7 PERST_N pin share scheme

Controlled by the PERST_ MODE register.

Pin Name	1'b0	1'b1
PERST_N	PERST_N	GPIO#36

2.3.8 WDT_RST_N pin share scheme

Controlled by the WDT _MODE register.

Pin Name	1'b0	1'b1
WDT_RST_N	WDT_RST_N	GPIO#37

2.3.9 REF_CLKO pin share scheme

Controlled by the REFCLK _MODE register.

Pin Name	1'b0	1'b1
REF_CLKO	REF_CLKO	GPIO#38

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2.3.10 UART0 pin share scheme

Controlled by the UART0 _MODE register.

Pin Name	1'b0	1'b1
UART_TXD0	UART_TXD0	GPIO#12
UART_TXD0	UART_RXD0	GPIO#13

2.3.11 GPIO0 pin share scheme

Controlled by GPIO_MODE register.

Pin Name	2'b00	2'b01	2'b10	2'b11
GPIO0	GPIO#11	GPIO#11	REF_CLKO	PERST_N

2.3.12 SPI pin share scheme

Controlled by SPI_ MODE register.

Pin Name	1'b0	1'b1
SPI_CLK	SPI_CLK	GPO#7
SPI_MOSI	SPI_MOSI	GPO#8
SPI_MISO	SPI_MISO	GPIO#9
SPI_CS0	SPI_CS0	GPIO#10

2.3.13 SPI_CS1 pin share scheme

Controlled by SPI_CS1_MODE register.

Pin Name	2'b00	2'b01	2'b10
SPI_CS1	SPI_CS1	GPIO#6	REF_CLKO

2.3.14 I2C pin share scheme

Controlled by I2C_MODE register.

Pin Name	2'b00	2'b01
I2C_SCLK	I2C_SCLK	GPIO#4
I2C_SD	I2C_SD	GPIO#5

2.3.15 I2S pin share scheme

Controlled by I2S_MODE register.

Pin Name	2'b00	2'b01	2'b10
I2S_SDI	I2C_SCLK	GPIO#0	PCMDRX
I2S_SDO	I2C_SD	GPIO#1	PCMDTX
I2S_WS	I2C_SCLK	GPIO#2	PCMCLK
I2S_CLK	I2C_SD	GPIO#3	PCMFS

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2.3.16 SD pin share scheme

Controlled by the EPHY_APGIO_AIO_EN[4:1] and SD_MODE registers

Pin Name	EPHY_APGIO_AIO_EN[4:1] =4'b0000	EPHY_APGIO_AIO_EN[4:1] =4'b1111	
		SD_MODE =2'b00	SD_MODE =2'b01
MDI_TP_P3	MDI_TP_P3	SD_WP	GPIO#22
MDI_TN_P3	MDI_TN_P3	SD_CD	GPIO#23
MDI_RP_P3	MDI_RP_P3	SD_D1	GPIO#24
MDI_RN_P3	MDI_RN_P3	SD_D0	GPIO#25
MDI_RP_P4	MDI_RP_P4	SD_CLK	GPIO#26
MDI_TN_P4	MDI_TN_P4	SD_D2	GPIO#27
MDI_RN_P4	MDI_RN_P4	SD_CMD	GPIO#28
MDI_TP_P4	MDI_TP_P4	SD_D3	GPIO#29

2.3.17 UART2 pin share scheme

Controlled by the EPHY_APGIO_AIO_EN[4:1] and UART2_MODE registers

	4'b0000	4'b1111			
Pin Name		2'b00	2'b01	2'b10	2'b11
MDI_TP_P2	MDI_TP_P2	UART_TXD2	GPIO#20	PWM_CH2	SD_D5
MDI_TN_P2	MDI_TN_P2	UART_RXD2	GPIO#21	PWM_CH3	SD_D4

2.3.18 PWM_CH0 pin share scheme

Controlled by the EPHY_APGIO_AIO_EN[4:1] and PWM0_MODE registers

	4'b0000	4'b1111			
Pin Name		2'b00	2'b01	2'b10	2'b11
MDI_RP_P2	MDI_RP_P2	PWM_CH0	GPIO#18		SD_D7

2.3.19 PWM_CH1 pin share scheme

Controlled by the EPHY_APGIO_AIO_EN[4:1] and PWM1_MODE registers

	4'b0000	4'b1111			
Pin Name		2'b00	2'b01	2'b10	2'b11
MDI_RN_P2	MDI_RN_P2	PWM_CH1	GPIO#19		SD_D6

2.3.20 SPIS pin share scheme

Controlled by the EPHY_APGIO_AIO_EN[4:1] and SPIS_MODE registers

	4'b0000	4'b1111			
Pin Name		2'b00	2'b01	2'b10	2'b11

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Pin Name	4’b0000	4’b1111 2’b00	2’b01	2’b10	2’b11
MDI_TP_P1	MDI_TP_P1	SPIS_CS	GPIO#14		PWM_CH0
MDI_TN_P1	MDI_TN_P1	SPIS_CLK	GPIO#15		PWM_CH1
MDI_RP_P1	MDI_RP_P1	SPIS_MISO	GPIO#16		UART_TXD2
MDI_RN_P1	MDI_RN_P1	SPIS_MOSI	GPIO#17		UART_RXD2

2.3.21 Pin share function description

Pin Share Name	I/O	Pin Share Function description
PCMDTX	O	PCM Data Transmit DATA signal sent from the PCM host to the external codec.
PCMDRX	I	PCM Data Receive DATA signal sent from the external codec to the PCM host.
PCMCLK	I/O	PCM Clock The clock signal can be generated by the PCM host (Output direction), or provided by an external clock (input direction). The clock frequency should match the slot configuration of the PCM host. e.g. 4 slots, PCM clock out/in should be 256 kHz. 8 slots, PCM clock out/in should be 512 kHz. 16 slots, PCM clock out/in should be 1.024 MHz. 32 slots, PCM clock out/in should be 2.048 MHz. 64 slots, PCM clock out/in should be 4.096 MHz. 128 slots, PCM clock out/in should be 8.192 MHz.
PCMFS	I/O	PCM SYNC signal. In our design, the direction of this signal is independent of the direction of PCMCLK. Its direction and mode is configurable.
PWM_CH0	O	Pulse Width Modulation Channle 0
PWM_CH1	O	Pulse Width Modulation Channle 1
PWM_CH2	O	Pulse Width Modulation Channle 2
PWM_CH3	O	Pulse Width Modulation Channle 3

2.4 Bootstrapping Pins Description

Pin Name	Boot Strapping Signal Name	Description
UART_TXD1	DBG_JTAG_MODE	0: JTAG_MODE 1: EPHY_LED (default)
PERST_N	XTAL_FREQ_SEL	0: 25 MHz DIP 1: 40 MHz SMD

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Pin Name	Boot Strapping Signal Name	Description
I2S_SDO	DRAM_TYPE	1: DDR1 0: DDR2 [note] This pin is valid for MT7628NN only. It needs to be pull-low for 7628KN which only supports DDR1.
{SPI_CS1 SPI_CLK, SPI_MOSI}	CHIP_MODE[2:0]	A vector to set chip function/test/debug modes. 000: Boot from PLL (boot from SPI 3-Byte Addr) 001: Boot from PLL (boot from SPI 4-Byte Addr) 010: Boot from XTAL (boot from SPI 3-Byte Addr) 011: Boot from XTAL (boot from SPI 4-Byte Addr)
PAD_TXD0	EXT_BGCK	1: Test Mode 0: Normal (default)

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3. Maximum Ratings and Operating Conditions

3.1 Absolute Maximum Ratings

I/O supply voltage	3.63 V
Input, Output, or I/O Voltage	GND -0.3 V to Vcc +0.3 V

Table 3-1 Absolute Maximum Ratings

3.2 Maximum Temperatures

Maximum Junction Temperature (Plastic Package)	125 °C
Maximum Lead Temperature (Soldering 10 s)	260 °C

Table 3-2 Maximum Temperatures

3.3 Operating Conditions

I/O supply voltage	3.3 V +/- 10%
DDR1 supply voltage	2.5 V +/- 5%
DDR2 supply voltage	1.8 V +/- 5%
Core supply voltage	1.2 V +/- 10%
Ambient Temperature Range	-20 to 55 °C

Table 3-3 Operating Conditions

3.4 Thermal Characteristics

Thermal characteristics without an external heat sink in still air conditions.

MT7628KN:

Thermal Resistance θ_{JA} (°C /W) for JEDEC 2L system PCB	26.1°C/W
Thermal Resistance θ_{JA} (°C /W) for JEDEC 4L system PCB	17.72°C/W
Thermal Resistance θ_{JC} (°C /W) for JEDEC	6.5°C/W
Thermal Resistance ψ_{Jt} (°C /W) for JEDEC 2L system PCB	1.81°C/W
Thermal Resistance ψ_{Jt} (°C /W) for JEDEC 4L system PCB	1.18°C/W

MT7628NN:

Thermal Resistance θ_{JA} (°C /W) for JEDEC 2L system PCB	27.01°C/W
Thermal Resistance θ_{JA} (°C /W) for JEDEC 4L system PCB	18.15°C/W
Thermal Resistance θ_{JC} (°C /W) for JEDEC	6.9°C/W
Thermal Resistance ψ_{Jt} (°C /W) for JEDEC 2L system PCB	2.41 °C/W
Thermal Resistance ψ_{Jt} (°C /W) for JEDEC 4L system PCB	1.51 °C/W

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Table 3-4 Thermal Characteristics

3.5 Storage Conditions

The calculated shelf life in a sealed bag is 12 months if stored between 0 °C and 40 °C at less than 90% relative humidity (RH). After the bag is opened, devices that are subjected to solder reflow or other high temperature processes must be handled in the following manner:

- Mounted within 168 hours of factory conditions, i.e. < 30 °C at 60% RH.
- Storage humidity needs to maintained at < 10% RH.
- Baking is necessary if the customer exposes the component to air for over 168 hrs, baking conditions: 125 °C for 8 hrs.

3.6 External Xtal Specfication

Frequency	25 MHz/ 40 Mhz
Frequency offset	+/-20 ppm
VIH/VIL	Vcc-0.3 V/0.3 V
Duty cycle	45% to 55%

Table 3-5 External Xtal Specifications

3.7 DC Electrical Characteristics

Parameters	Sym	Conditions	Min	Typ	Max	Unit
3.3 V supply voltage (IO)	Vddc33		2.97	3.3	3.63	V
2.5V supply voltage (DDR1)	Vdd25		2.375	2.5	2.625	V
1.8 V supply voltage (DDR2)	Vdd18		1.71	1.8	1.89	V
1.2 V supply voltage	Vdd12		1.08	1.2	1.32	V
3.3 V current consumption	Icc33					mA
1.5 V current consumption	Icc15					mA
1.2 V current consumption	Icc12					mA
DDR2 Current	Icc18					mA

Table 3-6 DC Electrical Characteristics

Vdd=2.5V (DDR2)	Min	Typ	Max
Vdd	2.375	2.5	2.625
VIH	VREF+0.15		Vdd25+0.3
VIL	-0.3		VREF-0.15
VOH	0.8*Vdd25		
VOL			0.2*Vdd25

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IOL			
IOH			

Table 3-7 Vdd 2.5V Electrical Characteristics

Vdd=1.8V (DDR2)	Min	Typ	Max
Vdd	1.71	1.8	1.89
VIH	VREF+0.125		Vdd18+0.3
VIL	-0.3		VREF-0.125
VOH	1.42		
VOL			0.28
IOL			
IOH			

Table 3-8 Vdd 1.8V Electrical Characteristics

Vdd=3.3V	Min	Typ	Max
Vdd	2.97V	3.3V	3.63V
VIH	2.0V		Vdd33+0.3
VIL	-0.3		0.8V
VOH	2.4V		
VOL			0.4V
IOL			
IOH			

Table 3-9 Vdd 3.3V Electrical Characteristics

3.8 AC Electrical Characteristics

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3.8.1 DDR2 SDRAM Interface

The DDR2 SDRAM interface complies with 200 MHz timing requirements for standard DDR2 SDRAM. The interface drivers are SSTL_18 drivers matching the EIA/JEDEC standard JESD8-15A.

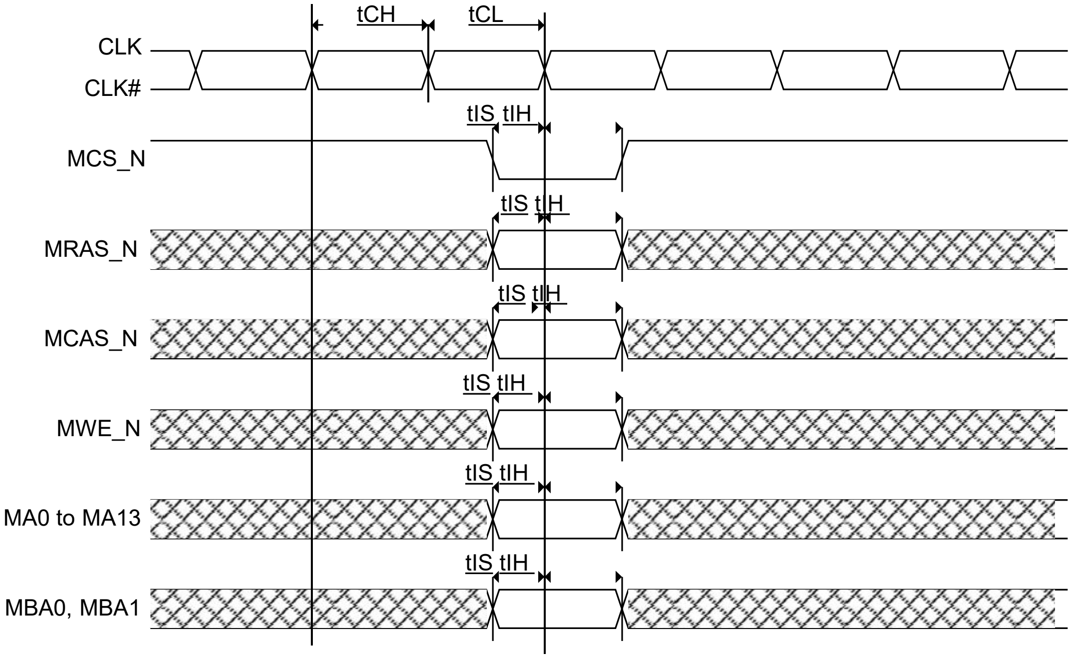

Figure 3-1 DDR2 SDRAM Command

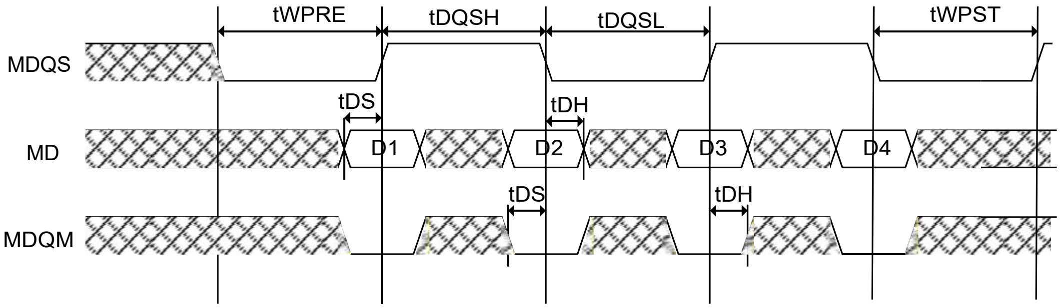

Figure 3-2 DDR2 SDRAM Write data

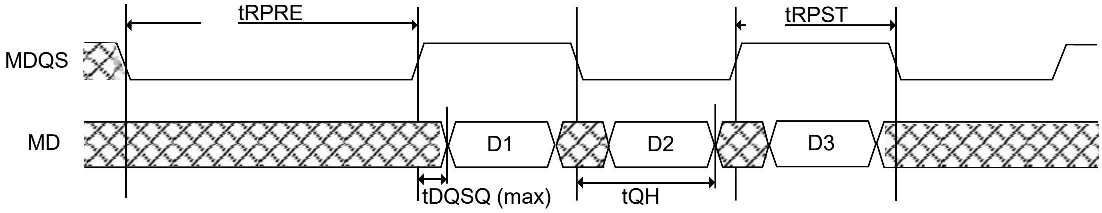

Figure 3-3 DDR2 SDRAM Read data

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Symbol	Description	Min	Max	Unit	Remark
tCK(avg)	Clock cycle time	5	-	ns	
tAC	DQ output access time from SDRAM CLK	-0.6	0.6	ns	
tDQSCK	DQS output access time from SDRAM CLK	-0.5	0.5	ns	
tCH	SDRAM CLK high pulse width	0.48	0.52	tCK(avg)	
tCL	SDRAM CLK low pulse width	0.48	0.52	tCK(avg)	
tHP	SDRAM CLK half period	Min(tCH,tCL)	-	ns	
tIS	Address and control input setup time	0.75	-	ns	
tIH	Address and control input hold time	0.75	-	ns	
tDQSQ	Data skew of DQS and associated DQ	-	0.4	ns	
tQH	DQ/DQS output hold time from DQS	tHP-0.5	-	ns	
tRPRE	DQS read preamble	0.9	1.1	tCK	
tRPST	DQS read postamble	0.4	0.6	tCK	
tDQSS	DQS rising edge to CK rising edge	-0.25	0.25	tCK	
tDQSH	DQS input-high pulse width	0.35	-	tCK	
tDQSL	DQS input-low pulse width	0.35	-	tCK	
tDSS	DQS falling edge to SDRAM CLK setup time	0.2	-	tCK	
tDSH	DQS falling edge hold time from SDRAM CLK	0.2	-	tCK	
tWPRE	DQS write preamble	0.35	-	tCK	
tWPST	DQS write postamble	0.4	0.6	tCK	
tDS	DQ and DQM input setup time	*0.4	-	ns	
tDH	DQ and DQM input hold time	*0.4	-	ns	

Table 3-10 DDR2 SDRAM Interface Diagram Key

NOTE: Depends on slew rate of DQS and DQ/DQM for single ended DQS.

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3.8.2 SPI Interface

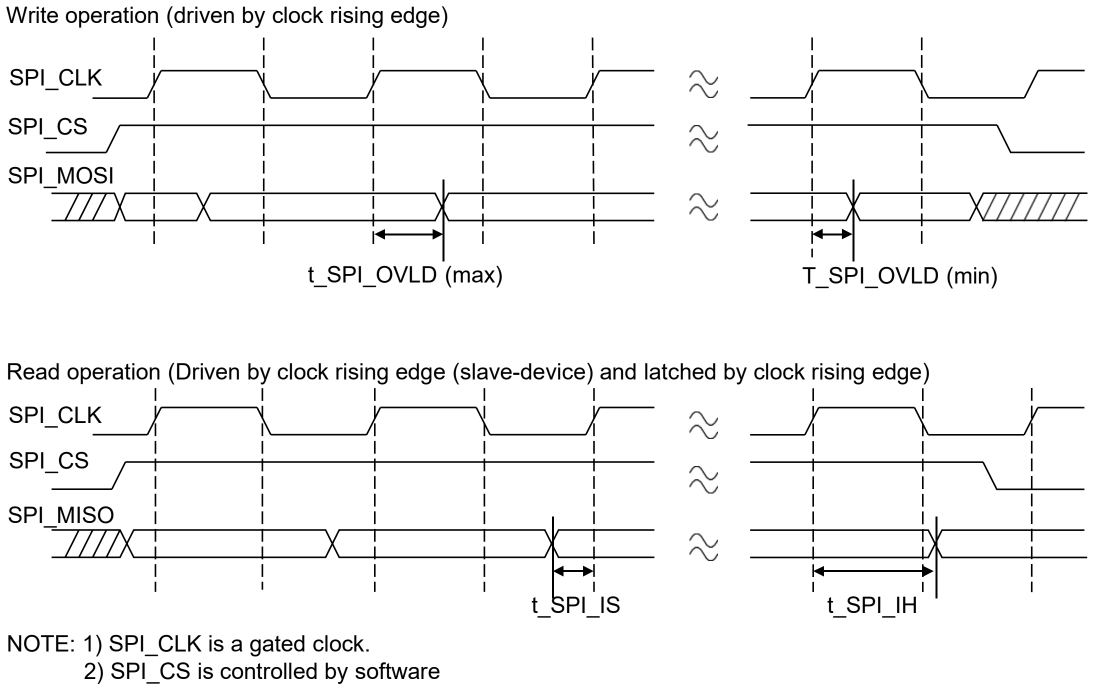

Figure 3-4 SPI Interface

Symbol	Description	Min	Max	Unit	Remark
t_SPI_IS	Setup time for SPI input	6.0	-	ns	
t_SPI_IH	Hold time for SPI input	-1.0	-	ns	
t_SPI_OVLD	SPI_CLK to SPI output valid	-2.0	3.0	ns	output load: 5 pF

Table 3-11 SPI Interface Diagram Key

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3.8.3 I²S Interface

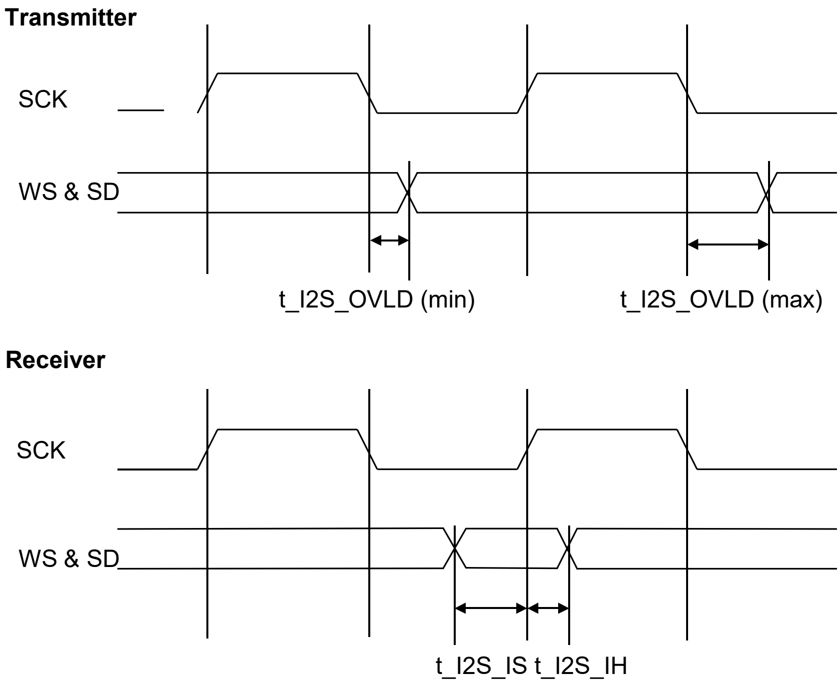

Figure-3-5 I2S Interface

Symbol	Description	Min	Max	Unit	Remark
t_I2S_IS	Setup time for I2S input (data & WS)	3.5	-	ns	
t_I2S_IH	Hold time for I2S input (data & WS)	0.5	-	ns	
t_I2S_OVLD	I2S_CLK to I2S output (data & WS) valid	2.5	10.0	ns	output load: 5 pF

Table 3-12 I2S Interface Diagram Key

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3.8.4 PCM Interface

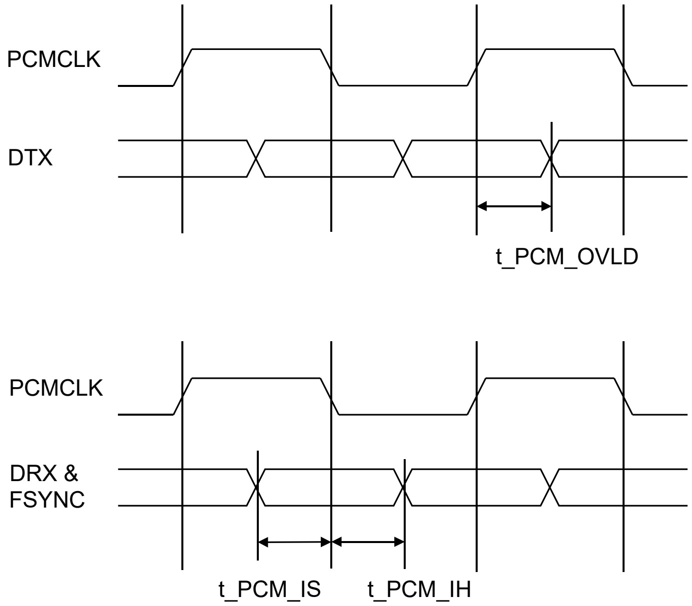

Figure 3-6 PCM Interface

Symbol	Description	Min	Max	Unit	Remark
t_PCM_IS	Setup time for PCM input to PCM_CLK fall	3.0	-	ns	
t_PCM_IH	Hold time for PCM input to PCM_CLK fall	1.0	-	ns	
t_PCM_OVLD	PCM_CLK rise to PCM output valid	10.0	35.0	ns	output load: 5 pF

Table 3-13 PCM Interface Diagram Key

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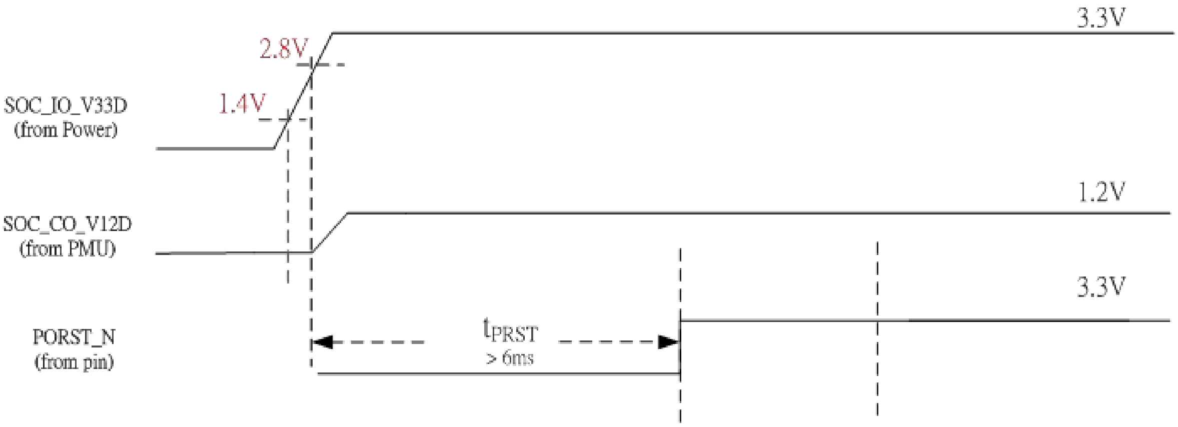
3.8.5 Power On Sequence



Symbol	Description	Min	Max	Unit
t_{PRST}	External Power-on Reset Period	6.0		ms

Figure 3-7 Power ON Sequence

Table 3-14 Power ON Sequence Diagram Key

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3.9 Package Physical Dimensions

3.9.1 DR-QFN (10 mm x 10 mm) 128 pins

3.9.1.1 Top View

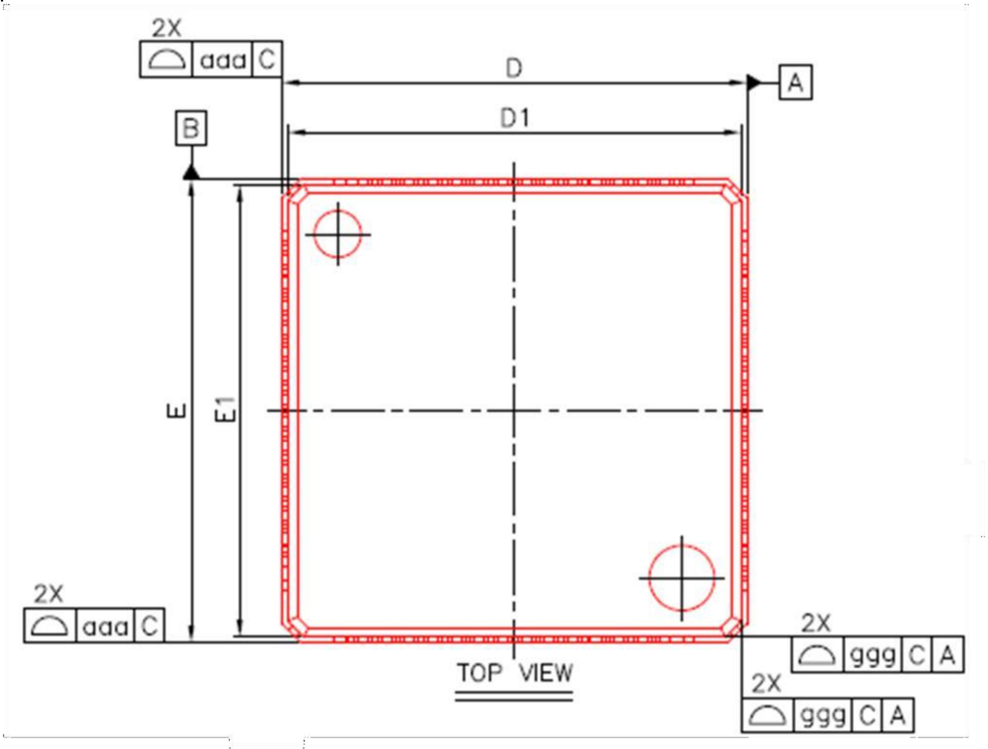

Figure 3-8 Top View

3.9.1.2 Side View

3.9.1.3 "B" Expanded

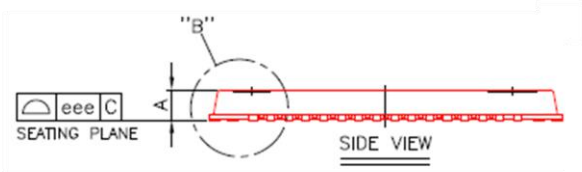

Figure 3-9 Side View

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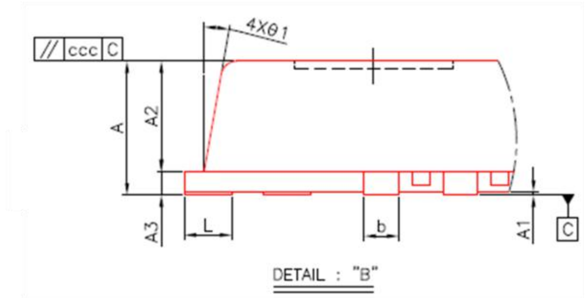

Figure 3-10 "B" Expanded

3.9.1.4 Bottom View

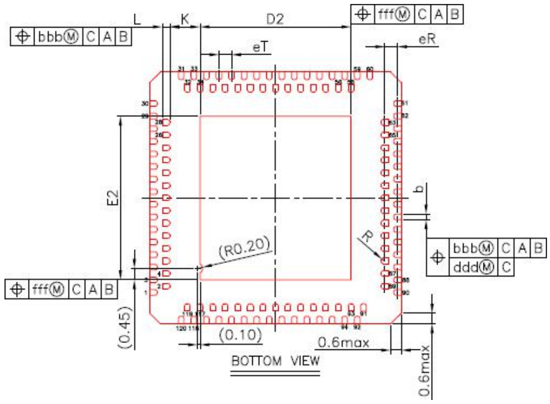

Figure 3-11 Botton view

3.9.1.5 Package Diagram Key

Item	SYMBOL	MIN.	NOM.	MAX.
TOTAL THICKNESS	A	0.80	0.85	0.90
LEAD STAND OFF.	A1	0.00	0.02	0.05
MOLD THICKNESS	A2	0.65	0.70	0.75
L/F THICKNESS	A3	0.15 REF.		
LEAD WIDTH	b	0.18	0.22	0.30
PACKAGE SIZE	D	9.90	10.00	10.10
	E			
Mold Edge size	D1	9.75 BSC		
	E1	9.75 BSC		
E-PAD size	D2	5.90	6.00	6.10
	E2	6.40	6.50	6.60
LEAD LENGTH	L	0.20	0.30	0.40
LEAD PITCH (BSC.)	eT	0.50 BSC		
LEAD PITCH (BSC.)	eR	0.50 BSC		
ANGLE	θ1	5°	---	15°
LEAD ARC	R	0.09	---	0.14
Lead to E-PAD Toler-ance	K	0.20	---	---
PKG EDGE TOLER-ANCE	aaa	0.10		
PACKAGE PROFILE OF A SURFACE	bbb	0.10		
LEAD PROFILE OF A SURFACE	ccc	0.10		
LEAD POSITION	ddd	0.05		
LEAD PROFILE OF A SURFACE	eee	0.08		
EPAD POSTION	fff	0.10		
Mold edge OF A & C SURFACE	ggg	0.20		

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3.9.2 DR-QFN (12 mm x 12 mm) 156 pins

3.9.2.1 Top View

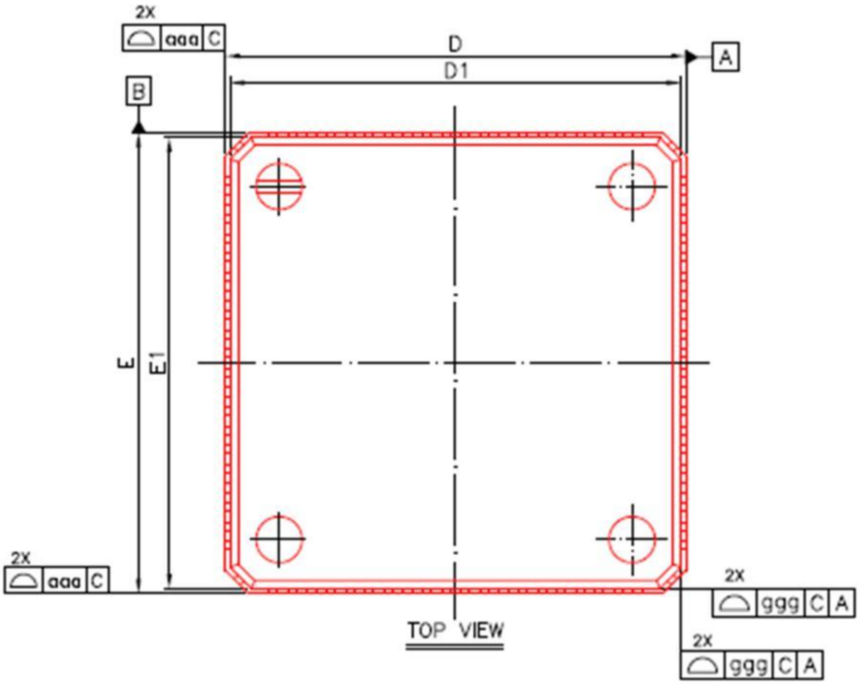

Figure 3-12 Top View

3.9.2.2 Side View

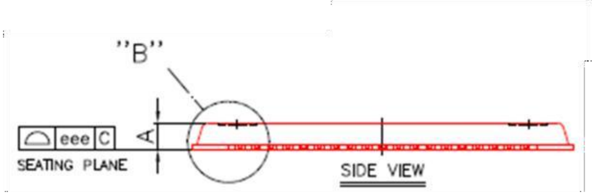

Figure 3-13 Side View

3.9.2.3 "B" Expanded

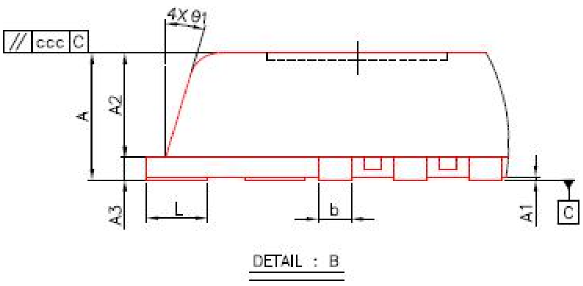

Figure 3-14 "B" Expanded

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3.9.2.4 Bottom View

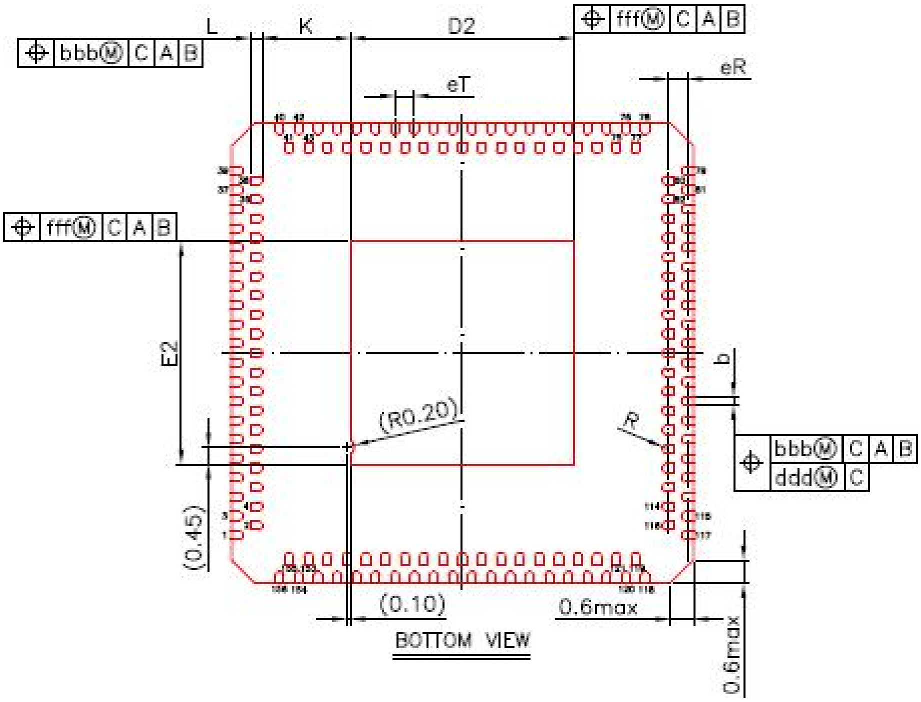

Figure 3-15 Bottom View

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3.9.2.5 Package Diagram Key

Item	SYMBOL	MIN.	NOM.	MAX.
TOTAL THICKNESS	A	0.80	0.85	0.90
LEAD STAND OFF.	A1	0.00	0.02	0.05
MOLD THICKNESS	A2	0.65	0.70	0.75
L/F THICKNESS	A3	0.15 REF.		
LEAD WIDTH	b	0.18	0.22	0.30
PACKAGE SIZE	D	11.90	12.00	12.10
	E			
Mold Edge size	D1	11.75 BSC		
	E1	11.75 BSC		
E-PAD size	D2	5.70	5.80	5.90
	E2	5.70	5.80	5.90
LEAD LENGTH	L	0.20	0.30	0.40
LEAD PITCH (BSC.)	eT	0.50 BSC		
LEAD PITCH (BSC.)	eR	0.50 BSC		
ANGLE	θ1	5°	---	15°
LEAD ARC	R	0.09	---	0.14
Lead to E-PAD Toler-ance	K	0.20	---	---
PKG EDGE TOLER-ANCE	aaa	0.10		
PACKAGE PROFILE OF A SURFACE	bbb	0.10		
LEAD PROFILE OF A SURFACE	ccc	0.10		
LEAD POSITION	ddd	0.05		
LEAD PROFILE OF A SURFACE	eee	0.08		
EPAD POSTION	fff	0.10		
Mold edge OF A & C SURFACE	ggg	0.20		

3.9.3 MT7628 AN/KN marking

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YYWW: Date code
LLLLLLLLL : Lot number
"."   : Pin #1 dot

Figure 3-16 MT7620AN top marking

YYWW: Date code
LLLLLLLLLL : Lot number
"."   : Pin #1 dot

Figure 3-17 MT7628KN top marking

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3.9.4 Reflow profile guideline

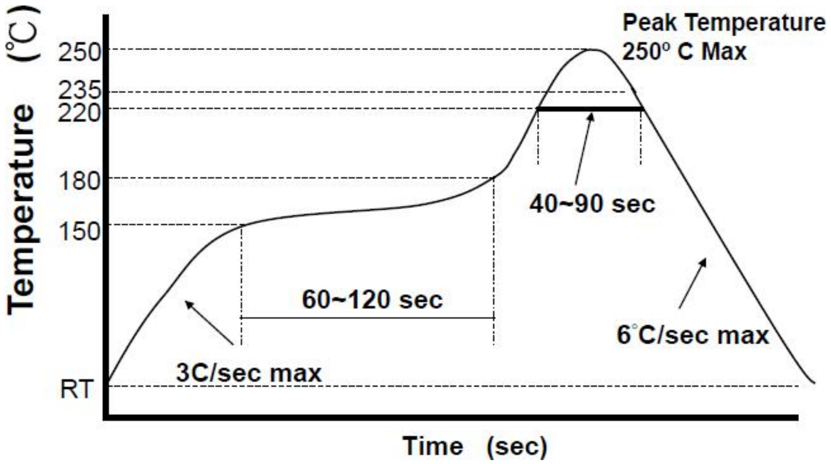

Figure 3-18 Reflow profile for MT7628

Notes;
1. Reflow profile guideline is designed for SnAgCulead-free solder paste.
2. Reflow temperature is defined at the solder ball of package/or the lead of package.
3. MTK would recommend customer following the solder paste vendor's guideline to design a profile appropriate your line and products.
4. Appropriate N2 atmosphere is recommended since it would widen the process window and mitigate the risk for having solder open issues.

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4. Abbreviations

Abbrev.	Description
AC	Access Category
ACK	Acknowledge/ Acknowledgement
ACPR	Adjacent Channel Power Ratio
AD/DA	Analog to Digital/Digital to Analog converter
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
AGC	Auto Gain Control
AIFS	Arbitration Inter-Frame Space
AIFSN	Arbitration Inter-Frame Spacing Number
ALC	Asynchronous Layered Coding
A-MPDU	Aggregate MAC Protocol Data Unit
A-MSDU	Aggregation of MAC Service Data Units
AP	Access Point
ASIC	Application-Specific Integrated Circuit
ASME	American Society of Mechanical Engineers
ASYNC	Asynchronous
BA	Block Acknowledgement
BAC	Block Acknowledgement Control
BAR	Base Address Register
BBP	Baseband Processor
BGSEL	Band Gap Select
BIST	Built-In Self-Test
BSC	Basic Spacing between Centers
BJT	
BSSID	Basic Service Set Identifier
BW	Bandwidth
CCA	Clear Channel Assessment
CCK	Complementary Code Keying
CCMP	Counter Mode with Cipher Block Chaining Message Authentication Code Protocol
CCX	Cisco Compatible Extensions
CF-END	Control Frame End
CF-ACK	Control Frame Acknowledgement
CLK	Clock

Abbrev.	Description
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
CSR	Control Status Register
CTS	Clear to Send
CW	Contention Window
CWmax	Maximum Contention Window
CWmin	Minimum Contention Window
DAC	Digital-To-Analog Converter
DCF	Distributed Coordination Function
DDONE	DMA Done
DDR	Double Data Rate
DFT	Discrete Fourier Transform
DIFS	DCF Inter-Frame Space
DMA	Direct Memory Access
DSP	Digital Signal Processor
DW	DWORD
EAP	Expert Antenna Processor
EDCA	Enhanced Distributed Channel Access
EECS	EEPROM chip select
EEDI	EEPROM data input
EEDO	EEPROM data output
EEPROM	Electrically Erasable Programmable Read-Only Memory
eFUSE	electrical Fuse
EESK	EEPROM source clock
EIFS	Extended Inter-Frame Space
EIV	Extend Initialization Vector
EVM	Error Vector Magnitude
FDS	Frequency Domain Spreading
FEM	Front-End Module
FEQ	Frequency Equalization
FIFO	First In First Out
FSM	Finite-State Machine
GF	Green Field
GND	Ground
GP	General Purpose
GPO	General Purpose Output
GPIO	General Purpose Input/Output

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Abbrev.	Description
HCCA	HCF Controlled Channel Access
HCF	Hybrid Coordination Function
HT	High Throughput
HTC	High Throughput Control
ICV	Integrity Check Value
IFS	Inter-Frame Space
iNIC	Intelligent Network Interface Card
IV	Initialization Vector
I^2C	Inter-Integrated Circuit
I^2S	Integrated Inter-Chip Sound
I/O	Input/Output
IPI	Idle Power Indicator
IQ	In phase/Quadrature phase
JEDEC	Joint Electron Devices Engineering Council
JTAG	Joint Test Action Group
kbps	kilo (1000) bits per second
KB	Kilo (1024) Bytes
LDO	Low-Dropout Regulator
LDODIG	LDO for DIGital part output voltage
LED	Light-Emitting Diode
LNA	Low Noise Amplifier
LO	Local Oscillator
L-SIG	Legacy Signal Field
MAC	Medium Access Control
MCU	Microcontroller Unit
MCS	Modulation and Coding Scheme
MDC	Management Data Clock
MDIO	Management Data Input/Output
MEM	Memory
MFB	MCS Feedback
MFS	MFB Sequence
MIC	Message Integrity Code
MIMO	Multiple-Input Multiple-Output
MLNA	Monolithic Low Noise Amplifier
MM	Mixed Mode
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MPDU	MAC Protocol Data Units
MSB	Most Significant Bit

Abbrev.	Description
NAV	Network Allocation Vector
NAS	Network-Attached Server
NAT	Network Address Translation
NDP	Null Data Packet
NVM	Non-Volatile Memory
ODT	On-die Termination
Oen	Output Enable
OFDM	Orthogonal Frequency-Division Multiplexing
OSC	Open Sound Control
PA	Power Amplifier
PAPE	Provider Authentication Policy Extension
PBC	Push Button Configuration
PBF	Packet Buffer
PCB	Printed Circuit Board
PCF	Point Coordination Function
PCM	Pulse-Code Modulation
PHY	Physical Layer
PIFS	PCF Interframe Space
PLCP	Physical Layer Convergence Protocol
PLL	Phase-Locked Loop
PME	Physical Medium Entities
PMU	Power Management Unit
PN	Packet Number
PROM	Programmable Read-Only Memory
PSDU	Physical layer Service Data Unit
PSI	Power supply Strength Indication
PSM	Power Save Mode
PTN	Packet Transport Network
QoS	Quality of Service
RDG	Reverse Direction Grant
RAM	Random Access Memory
RF	Radio Frequency
RGMII	Reduced Gigabit Media Independent Interface
RH	Relative Humidity
RoHS	Restriction on Hazardous Substances
ROM	Read-Only Memory

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Abbrev.	Description
RSSI	Received Signal Strength Indication (Indicator)
RTS	Request to Send
RvMII	Reverse Media Independent Interface
Rx	Receive
RXD	Received Data
RXINFO	Receive Information
RXWI	Receive Wireless Information
S	Stream
SDXC	Secure Digital eXtended Capacity
SDIO	Secure Digital Input Output
SDRAM	Synchronous Dynamic Random Access Memory
SEC	Security
SGI	Short Guard Interval
SIFS	Short Inter-Frame Space
SoC	System-on-a-Chip
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SSCG	Spread Spectrum Clock Generator
STBC	Space–Time Block Code
SW	Switch Regulator
TA	Transmitter Address
TBTT	Target Beacon Transmission Time
TDLS	Tunnel Direct Link Setup
TKIP	Temporal Key Integrity Protocol
TRSW	Tx/Rx Switch
TSF	Timing Synchronization Function

Abbrev.	Description
TSSI	Transmit Signal Strength Indication
Tx	Transmit
TxBF	Transmit Beamforming
TXD	Transmitted Data
TXDAC	Transmit Digital-Analog Converter
TXINFO	Transmit Information
TXOP	Opportunity to Transmit
TXWI	Tx Wireless Information
UART	Universal Asynchronous Rx/ Tx
USB	Universal Serial Bus
UTIF	Universal Test Interface
VGA	Variable Gain Amplifier
VCO	Voltage Controlled Amplifier
VIH	High Level Input Voltage
VIL	Low Level Input Voltage
VoIP	Voice over IP
WCID	Wireless Client Identification
WEP	Wired Equivalent
WI	Wireless Information
WIV	Wireless Information Valid
WMM	Wi-Fi Multimedia
WPA	Wi-Fi Protected Access
WPDMA	Wireless Polarization Division Multiple Access
WS	Word Select

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5. Revision History

Rev	Date	Description
1.0	2012/07/09	Initial Release
1.1	2012/07/18	Update SPI_WP/SPI_HOLD GPO table
1.2	2012/08/20	Fix DRQFN internal pad size typo
1.3	2012/09/12	Add IR reflow guideline

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